FPGA IMPLEMENTATION OF RECONFIGURABLE ARCHITECTURE FOR LOGICAL APPLICATIONS

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ABSTRACT

Coarse-Grained Reconfigurable Architecture (CGRAs) requires many Processing Elements (PEs) and a configuration cache memory unit for reconfiguration of its PE array. This structure is meant for high performance and flexibility, it consumes significant power. The applications of Field Programmable Gate Arrays (FPGAs) are multi fold in real-time systems. They have several advantages over Application Specific Integrated Circuits (ASICs), but CGRAs applications have been restricted to integer arithmetic, since existing CGRAs supports only integer arithmetic or logical applications. In this work proposed here main objective is to design existing 4 x 4 Processing Elements (PEs) array for integer arithmetic. The main idea of this paper is to explore the advantages of FPGA in real world by mapping applications that supports integer arithmetic and the mapping can be done by using the Fast Heuristic algorithm to get the required results. The focus is to do synthesis of both existing 4 x 4 PE array design and modified 4 x 4 PE array design for speed, power and delay using Xilinx and Xpower analysis tool. This design uses HDL, Modelsim simulator and Xilinx9.1i Synthesizer targeted on Vertex platform. Heuristic approach using Quantum- inspired Evolutionary Algorithm (QEA) used here supports for integer arithmetic applications. The proposed Modified Processing Elements proves to be 20 - 25% reduction in delay and power dissipation, when compared to the existing PEs of 4 x 4 elements. The proposed PEs might lead a significant reduction in power and delay when used in multimedia application, with maximum throughput.

KEYWORDS: Coarse-Grained Reconfigurable Architecture, Heuristic Approach, Processing Elements, Modified Quantum-Inspired Evolutionary Algorithm (QEA)